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Abstract: This paper presents a modified design of Area-Efficient Low power Carry Select Adder (CSLA) Circuit. In digital adders, the speed of addition is limited by the time required to transmit a carry through the adder. Carry select adder processors and systems. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The major speed limitation in any adder is in the production of carries.

Index terms: Area-efficient, Low power, CSLA, Binary to excess one converter, Multiplexer.

I. INTRODUCTION

conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path. However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder

to excess-1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure. the basic idea of the proposed work is by using n-bit binary to excess-1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure.

II. DELAY AND AREA EVALUATION OF THE BASIC ADDER BLOCKS

to excess-1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure. and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum

delay. The area evaluation is done by counting the total number of AOI gates required for each logic block.

Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

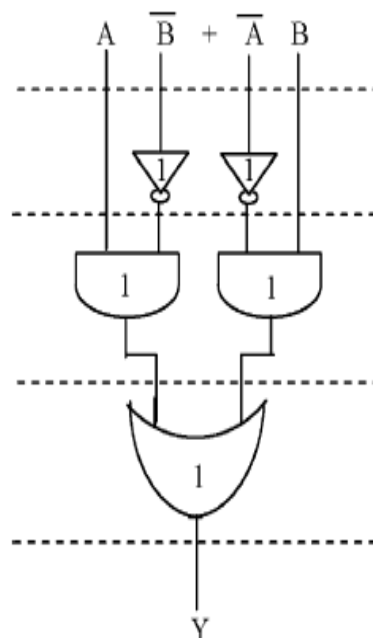


Figure 1: Delay and Area evaluation of an XOR gate.

Table 1
Delay and Area Evaluation of the Basic Blocks of CSLA

| Basic Blocks | Delay | Area |
|--------------|-------|------|
| XOR | 3 | 5 |
| 2:1 MUX | 3 | 4 |
| Half Adder | 3 | 6 |
| Full Adder | 6 | 13 |

III. BASIC STRUCTURE OF BEC LOGIC

conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path.

However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function table of a 4-bit BEC are shown in Figure.2 and Table .2, respectively.

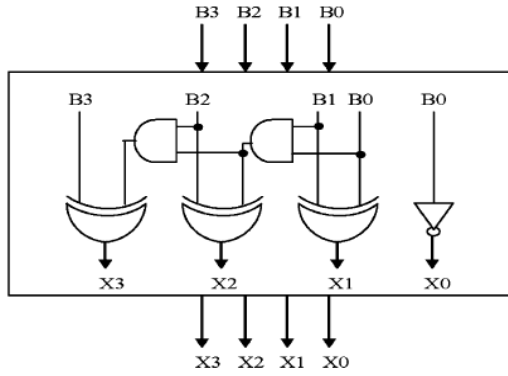


Figure 2: 4-Bit BEC

The Boolean expressions of the 4-bit BEC are

$$\begin{aligned} X0 &= \sim B0 & (1) \\ X1 &= B0 \wedge B1 & (2) \\ X2 &= B2 \wedge (B0 \wedge B1) & (3) \\ X3 &= B3 \wedge (B0 \wedge B1 \wedge B2) & (4) \end{aligned}$$

Table.2 Function table of the 4-bit BEC

| B[3:0] | X[3:0] |
|--------|--------|
| 0000 | 0001 |
| 0001 | 0010 |
| | |
| | |
| 1110 | |
| 1111 | 1111 |
| | 0000 |

IV. BASIC STRUCTURE OF REGULAR 16-BIT CSLA

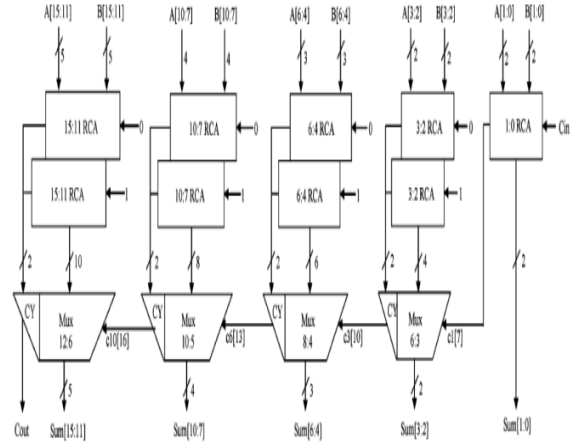


Figure 3: Regular CSLA circuit

The structure of the 16-b regular Sqrt CSLA conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path.

However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder

$$\{c6, \text{sum}[6:4]\} = c3[t=10] + \text{mux} \quad (5)$$

$$\{c10, \text{sum}[10:7]\} = c6[t=13] + \text{mux} \quad (6)$$

$$\{\text{Cout}, \text{sum}[15:11]\} = c10[t=16] + \text{mux}. \quad (7)$$

3) The one set of 2-b RCA in group2 has 2 FA for Cin=1 and the other set has 1 FA and 1 HA for Cin=0. Based on the area count of Table I, the total number of gate counts in group2 is determined as follows:

$$\text{Gate Count} = 57 \text{ (FA+HA+MUX)} \quad (8)$$

$$\text{FA} = 39(3*13) \quad (9)$$

$$\text{HA} = 6(1*6) \quad (10)$$

$$\text{MUX} = 12(3*4) \quad (11)$$

4) Similarly, the estimated maximum delay and area of the other groups in the regular Sqrt CSLA are evaluated and listed in Table 3.

Table 3

| Group | Delay | Area |
|-------|-------|------|
| 2 | 11 | 57 |
| 3 | 13 | 87 |
| 4 | 16 | 117 |
| 5 | 19 | 147 |

CONCLUSION

A to excess-1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure. is therefore, low area, low power, simple and efficient for VLSI hardware implementation.

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